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(54) [Title of the Invention] LIQUID CRYSTAL DISPLAY DEVICE

(57) [Abstract]

[Task] To reduce a speck of brightness in a display panel of an aperture-ratio active matrix type liquid crystal display device with high resolution in a liquid crystal display device.

[Configuration] A pixel electrode 2 is disposed to partly overlap with an n-th signal line 4 and a (n+1)-th signal line 4, and one division counter electrode 5 is provided for at least one pixel. An external signal power source for applying a common voltage to the division counter electrode 5 only when being applied with a scan voltage and applying a signal pulse for floating the division counter electrode 5 to the division counter electrode in other cases is provided.

[Claims]

[Claim 1]

An active matrix type liquid crystal display device comprising:

a pixel electrode which overlaps with at least a part of an n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line;

a division counter electrode which is provided for at least one pixel; and

an external signal power source which applies a common voltage to the division counter electrode in case of being applied with a scan voltage and which applies a signal pulse for floating the division counter electrode to the division counter electrode in other cases.

[Claim 2]

An active matrix type liquid crystal display device comprising:

a pixel electrode which overlaps with at least a part of an n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line;

a stripe-shaped counter electrode which is provided for a pixel on a scan line; and

an external signal power source which sets a period during which a common voltage is applied to the stripe-shaped counter electrode to the product of the number of scan lines grouped

by the stripe-shaped counter electrode and one horizontal period and which applies a signal pulse for floating the stripe-shaped counter electrode to the striped shaped counter electrode in other cases.

[Claim 3]

The active matrix type liquid crystal display device according to Claim 1 or 2, wherein an element for switching the pixel is amorphous silicon TFT, and

wherein a scan driving circuit and a signal driving circuit for driving the amorphous silicon TFT are provided outside a TFT substrate and an opposite substrate.

[Claim 4]

An active matrix type liquid crystal display device comprising:

a pixel electrode which overlaps with at least a part of an n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line;

a bus line which is opposite each of the signal lines with the pixel electrode interposed therebetween and which is capacitive-coupled to the pixel electrode; and

means for applying to the bus line with a signal with polarity opposite to that of a signal which is applied to each of the signal lines opposite the bus line.

[Claim 5]

An active matrix type liquid crystal display device

comprising:

a pixel electrode which overlaps with a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line;

a conductive thin film which is disposed between the pixel electrode and at least one of the n-th signal line and the (n+1)-th signal line to be capacitive-coupled to the pixel electrode; and

means for applying to the conductive thin film with a signal with polarity opposite to that of a signal which is applied to the signal line on the opposite side to a side where the conductive thin film is provided.

[Claim 6]

An active matrix type liquid crystal display device comprising:

a pixel electrode which overlaps with at least a part of an n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line, wherein each of the signal lines is coated with a high-resistance thin film.

[Claim 7]

An active matrix type liquid crystal display device comprising:

a pixel electrode which overlaps with at least a part of a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line, wherein each of the signal lines is formed in an inverted mesa shape in a sectional view to electrically

separate the pixel electrode on each of the signal lines from the pixel electrode provided between the signal lines.

[Claim 8]

The active matrix type liquid crystal display device according to Claim 7, wherein a conductive film which extends in the same direction as that of the signal lines is provided below each of the signal lines.

[Claim 9]

An active matrix type liquid crystal display device comprising:

a pixel electrode which overlaps with at least a part of a n-th scan line and a (n+1)-th scan line adjacent to the n-th scan line, wherein each of the scan lines is formed in an inverted mesa shape in a sectional view to electrically separate the pixel electrode on each of the scan lines from the pixel electrode provided between the scan lines.

[Claim 10]

The active matrix type liquid crystal display device according to Claim 9, wherein an auxiliary capacitance bus line which is formed of a conductive layer on the same layer of each of the scan lines and which has a rectangular shape or a mesa shape in a sectional view is provided between the n-th signal line and a (n+1)-th scan line adjacent to the n-th signal line.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Application]

The present invention relates to a liquid crystal display device, and more particularly, to an active matrix type liquid crystal display device, which reduces a speck of brightness, used for an OA terminal or a projector.

[0002]

[Prior Art]

In the past, a liquid crystal display device was used for an OA terminal or a projector due to a small size, light weight, and low power consumption, or a small-sized LCD TV etc. due to portability. In the apparatuses, an improvement of display performance and low power consumption are demanded.

[0003]

In order to realize low power consumption in the apparatuses, it is necessary to improve light use efficiency of back light. Accordingly, a pixel aperture ratio (aperture area of black matrix / occupying area of one pixel) in a liquid crystal panel needs to be improved.

[0004]

For example, in a panel used for a liquid crystal projector, the size of the panel is small such that the symmetric angle is about 7.6 cm (~ 3 inch). However, the same resolution as that of the liquid crystal display device used for the OA terminal in which the symmetric angle is about 25.4 cm (~ 10 inch) is demanded. For this reason, a pitch of one pixel is necessarily

small, but when the pitch of the pixel is made small in a panel of which an area is smaller than that of the liquid crystal display device used for the OA terminal in this way, a problem of positioning precision arises, and thus it is difficult to obtain a required resolution.

[0005]

The reason is described with reference to Fig. 10 (in the drawing, one pixel is shown), which is a top view showing a pixel configuration of the known liquid crystal display device.

See Fig. 10.

In the pixel of the known liquid crystal display device, on a TFT substrate 11, a signal line (data bus line) 12 and a scan line (gate bus line) 13 are provided so as to intersect each other. A semiconductor layer formed of amorphous silicon or polycrystalline silicon connected to the signal line 12 and a gate electrode 14 connected to the scan line are provided. Accordingly, a TFT for switching the pixel is formed. A pixel electrode 17 connected to a source 16 (Reference Numeral 15 denotes a drain) of the TFT is provided.

[0006]

In this case, a light shielding film such as a black matrix is provided on an opposite substrate. An area surrounded by a boundary 38 of the light shielding film shown by the dashed line in the drawing is referred to as a display aperture portion. However, in the liquid crystal display device, positioning

precision in the TFT substrate, that is, a margin a necessary for the positioning of each electrode etc. during a photolithography process is in the range of 3 to 5 μm. Additionally, positioning precision in the opposite substrate to the TFT substrate, that is, a margin b necessary at the time of attaching the opposite substrate to the TFT substrate is about ~ 7 μm. Accordingly, it is difficult to increase the pixel aperture ratio in accordance with miniaturization of the pixel pitch. Additionally, in this case, the width d_1 of the signal line 12 and the width d_2 of the scan line 13 are about 10 μm, respectively.

[0007]

In order to solve the problems, a method of providing the light shielding film such as a black matrix which was provided on the opposite substrate on the TFT substrate has been proposed. In this case, a problem of positioning precision between the TFT substrate and the opposite substrate does not occur. However, a problem arises in that it is difficult to position the light shielding film on the TFT substrate to other electrodes or it is difficult to conduct the process of forming the light shielding film. Thus, the improvement of the pixel aperture ratio was not realized as expected.

[0008]

As another improvement, as shown in Fig. 11, an aperture-ratio liquid crystal display device with high

resolution in which the pixel electrode 17 overlaps with the signal line 12 so as to allow the signal line 12 to function as the light shielding film has been proposed. Additionally, Fig. 11(a) is a top view (in the drawing, one pixel unit is shown) illustrating the pixel configuration on the TFT substrate. Fig. 11(b) is a sectional view taken along the dashed line A-A' shown in Fig. 11(a).

[0009]

See Figs. 11(a) and 11(b).

In the pixel of the aperture-ratio liquid crystal display device with high resolution, similarly to Fig. 10, on the TFT substrate 11, the signal line 12 and the scan line 13 are provided to intersect each other with the first interlayer insulation film 26 such as a SiO_2 film interposed therebetween. A semiconductor layer formed of amorphous silicon or polycrystalline silicon connected to the signal line 12 and a gate electrode 14 connected to the scan line are provided. Accordingly, a TFT for switching the pixel is formed.

[0010]

Subsequently, a second interlayer insulation film 27 such as a SiO_2 film is provided to cover the signal line 12, and then a conductive film such as ITO is deposited. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12 of the pixel and the signal line 12 of the adjacent

pixel is formed.

[0011]

In this case, since the signal line 12 of the pixel and the signal line 12 of the adjacent pixel are used as the light shielding film, a side where the signal line 12 of the pixel and the signal line 12 of the adjacent pixel are opposite each other forms a part of the boundary 38 of the light shielding film along the extension direction of the signal line 12. The opposite side, the light shielding film such as a black matrix provided on the opposite substrate forms the other part of the boundary 38 of the light shielding film along the extension direction of the scan line 13, that is, a direction where the signal line 12 is disposed.

[0012]

Likewise, in the pixel aperture defined by the boundary 38 of the light shielding film shown by the dashed line in Fig. 11, the whole pixel pitch except for the width of the signal line 12 is referred to as the aperture portion in the direction where the signal line 12 is disposed, it is possible to highly improve the pixel aperture ratio.

[0013]

[Problems that the Invention is to Solve]

However, in the aperture-ratio liquid crystal display device with high resolution shown in Fig. 11, a problem arises in that a speck of brightness occurs. The problem will be

described with reference to Fig. 12. Additionally, Fig. 12(a) shows an equivalent circuit to that of the pixel units in the aperture-ratio liquid crystal display device with high resolution shown in Fig. 11. Additionally, Fig. 12(b) is a view illustrating a potential variation in each signal waveform and each point at a driving time.

[0014]

See Fig. 12(a).

The pixel connected to the n-th signal line n includes a TFT as a switching element and a pixel capacitance C_{pix} having a pixel electrode P_n - liquid crystal - counter electrode. However, in actual, parasitic capacitances C_{Pn} and C_{Pn+1} are respectively formed in an overlap portion between the pixel electrode P_n and the signal line n and an overlap portion between the pixel electrode P_n and the signal line n+1 of an adjacent pixel. Additionally, the V_{COM} shown in the drawing is a common voltage applied to the counter electrode, and the parasitic capacitance is formed between the gate electrode connected to the scan line and the source of the TFT.

[0015]

See Fig. 12(b).

In the pixel with such a configuration, when a scan signal is applied to the scan line while the signal voltage is applied to the signal line n to turn on the TFT connected to the pixel electrode P_n, the pixel potential becomes V_{Pn}. At this time,

the pixel capacitance C_{pix} is charged with a charge Q_{pix} [$=C_{pix} \times (V_{Pn} - V_{COM})$, also, $V_{Pn} - V_{COM}$ denotes a liquid crystal voltage] by the signal voltage of the signal line n. Subsequently, the scan signal is turned off and then the TFT is turned off. The pixel capacitance C_{pix} is separated from the signal line n and then maintained in a charged state. Additionally, in this case, in accordance with the parasitic capacitance between the gate electrode and the source of the TFT, the pixel potential decreases by ΔV_{GS} by the same reason of the variation in the pixel potential described below. Hereinafter, the pixel potential which decreases by ΔV_{GS} is referred to as V_{Pn}.

[0016]

Subsequently, when the signal voltage of the signal line n is inverted to a minus, the pixel potential V_{Pn} decreases by ΔV_P in accordance with the signal voltage variation ΔV_d. That is, in accordance with the invert of the signal voltage, the parasitic capacitance C_{Pn} of the overlap portion of the pixel electrode P_n and the signal line n is connected to the pixel capacitance C_{pix} charged with the charge Q_{pix}. Accordingly, a part of the Q_{pix} moves to the parasitic capacitance C_{Pn} and the charge keeps moving until the state where the pixel potential is stabilized at a new pixel potential V'_{Pn} $(= V_{Pn} - \Delta V_P)$.

[0017]

The parasitic capacitance C_{Pn} is charged with a charge $Q_{par} = C_{Pn} \times (\Delta V_d - \Delta V_P)$ is charged. Additionally, on the basis

of law of conservation of charge, $Q_{pix} = Q'_{pix} + Q_{par}$. Thus, the potential variation in the pixel potential ΔV_P is $\Delta V_P = V_{Pn} - V'_{Pn} = Q_{pix} / C_{pix} - Q'_{pix} / C_{pix} = 1 / C_{pix} \times (Q_{pix} - Q'_{pix}) = Q_{par} / C_{pix} = C_{Pn} \times (\Delta V_d - \Delta V_P) / C_{pix}$.

When this expression solved, $\Delta V_P \times C_{pix} = C_{Pn} \times (\Delta V_d - \Delta V_P)$.

Therefore, $(C_{Pn} + C_{pix}) \Delta V_P = C_{Pn} \times \Delta V_d$, and thus $\Delta V_P = [C_{Pn} / (C_{Pn} + C_{pix})] \times \Delta V_d$.

[0018]

In accordance with the pixel potential variation ΔV_P, the liquid crystal voltage $(V_{Pn} - V_{COM})$ decreases to the same extent. Additionally, when the following scan signal is applied, since the signal voltage is a minus, a reverse direction charge occurs. When the signal voltage is inverted to a plus, the pixel potential increases by ΔV_P by the same reason described above and the liquid crystal voltage decreases by ΔV_P. The pixel potential variation ΔV_P is influenced by the voltage variation in the signal line n and the voltage variation in the signal line n+1 of the adjacent pixel.

[0019]

Next, a case where the variation in the voltage V_{dn} of the signal line n and the variation in the voltage V_{dn+1} of the signal line n+1 are inverted phases will be described with reference to Fig. 13.

See Fig. 13.

In the same manner as Fig. 12, when a scan voltage is

applied to the scan line while the signal voltage V_{dn} is applied to the signal line n to turn on the TFT connected to the pixel electrode P_n, the pixel potential becomes V_{Pn}. At this time, the pixel capacitance C_{pix} is charged with the signal voltage V_{dn} of the signal line n. Subsequently, the scan signal is turned off and then the TFT is turned off. The pixel capacitance C_{pix} is separated from the signal line n and then maintained in a charged state. Additionally, in this case, in accordance with the parasitic capacitance between the gate electrode and the source of the TFT, the pixel potential slightly decreases.

[0020]

Subsequently, when the voltage V_{dn} of the signal line n and the voltage V_{dn+1} of the signal line n+1 are changed to an inverted phase at the same time, directions of the variation ΔV_{Pn} of the signal voltage V_{dn} and the variation ΔV_{Pn+1} of the signal voltage V_{dn+1} are opposite to each other to be offset. In particular, when the magnitude of the parasitic capacitance C_{Pn} of the signal line n is the same as that of the parasitic capacitance C_{Pn+1} of the signal line n+1, and the absolute value of the voltage V_{dn} is the same as that of the voltage V_{dn+1}, $\Delta V_{Pn} = -\Delta V_{Pn+1}$ and the potential variation is completely offset. Accordingly, a variation in display brightness does not occur.

[0021]

Next, a case where the variation in the voltage V_{dn} of the signal line n and the variation in the voltage V_{dn+1} of the

signal line n+1 are the same phases will be described with reference to Fig. 14.

See Fig. 14.

In this case, in the same manner as Fig. 13, when a scan voltage is applied to the scan line while the signal voltage V_{dn} is applied to the signal line n to turn on the TFT connected to the pixel electrode P_n, the pixel potential becomes V_{Pn}. At this time, the pixel capacitance C_{pix} is charged with the signal voltage V_{dn} of the signal line n. Subsequently, the scan signal is turned off and then the TFT is turned off. The pixel capacitance C_{pix} is separated from the signal line n and then maintained in a charged state.

[0022]

Subsequently, when the voltage V_{dn} of the signal line n and the voltage V_{dn+1} of the signal line n+1 are changed to the same phase at the same time, directions of the variation ΔV_{Pn} by the signal voltage V_{dn} and the variation ΔV_{Pn+1} by the signal voltage V_{dn+1} are the same to each other to emphasize the variation. Accordingly, the pixel potential largely varies, and thus the liquid crystal voltage decreases.

[0023]

In this case, when a display of uniform brightness is intended to be carried out, a fluctuation of brightness occurs since the liquid crystal potential before and after the variation in the signal voltage is different. Additionally, when the

voltage variation of the same phase and the voltage variation of the inverted phase in the signal lines adjacent to each other occur in the panel of the liquid crystal display device, for example, at the time of a black display, areas where the liquid crystal voltage substantially decreases and does not decrease are generated. Accordingly, the voltage difference is recognized as a speck of brightness.

[0024]

Accordingly, an object of the invention is to remove a speck of brightness in a display panel of an aperture-ratio active matrix type liquid crystal display device with high resolution.

[0025]

[Means for Solving the Problems]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode (Reference Numeral 17 shown in Fig. 2) which overlaps with at least a part of a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line; one division counter electrode (Reference Numeral 25 shown in Fig. 2) which is provided for at least one pixel; and an external signal power source which applies a common voltage to the division counter electrode in case of being applied with a scan voltage and which applies a signal pulse for floating the division counter electrode to the division counter electrode in other cases.

[0026]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode which overlaps with at least a part of a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line; a stripe-shaped counter electrode (Reference Numeral 32 shown in Fig. 3) which is provided for a pixel on a scan line; and an external signal power source which sets a period during which a common voltage is applied to the stripe-shaped counter electrode to the product of the number of scan lines grouped by the stripe-shaped counter electrode and one horizontal period and which applies a signal pulse for floating the stripe-shaped counter electrode to the striped shaped counter electrode in other cases.

[0027]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode (Reference Numeral 17 shown in Fig. 5) which overlaps with at least a part of a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line; a bus line (Reference Numeral 40 shown in Fig. 5) which is opposite each of the signal lines (Reference Numeral 12 shown in Fig. 5) with the pixel electrode interposed therebetween and which is capacitive-coupled to the pixel electrode; and means for applying to the bus line with a signal with polarity opposite

to that of a signal which is applied to each of the signal lines opposite the bus line.

[0028]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode (Reference Numeral 17 shown in Fig. 6) which overlaps with a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line; a conductive thin film (Reference Numeral 41 shown in Fig. 6) which is disposed between the pixel electrode and at least one of the n-th signal line (Reference Numeral 12 shown in Fig. 6) and the (n+1)-th signal line (Reference Numeral 12 shown in Fig. 6) to be capacitive-coupled to the pixel electrode; and means for applying to the conductive thin film with a signal with polarity opposite to that of a signal which is applied to the signal line on the opposite side to a side where the conductive thin film is provided.

[0029]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode (Reference Numeral 17 shown in Fig. 6) which overlaps with at least a part of an n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line, wherein each of the signal lines (Reference Numeral 12 shown in Fig. 6) is coated with a high-resistance thin film (Reference Numeral 43 shown in Fig. 6).

[0030]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode (Reference Numeral 17 shown in Fig. 7) which overlaps with at least a part of a n-th signal line and a (n+1)-th signal line adjacent to the n-th signal line, wherein each of the signal lines (Reference Numeral 12 shown in Fig. 7) is formed in an inverted mesa shape in a sectional view to electrically separate the pixel electrode on each of the signal lines from the pixel electrode provided between the signal lines. According to the invention, a conductive film (Reference Numeral 46 shown in Fig. 7) which extends in the same direction as that of the signal lines is provided below each of the signal lines (Reference Numeral 12 shown in Fig. 7).

[0031]

According to the invention, there is provided an active matrix type liquid crystal display device including a pixel electrode (Reference Numeral 17 shown in Fig. 8) which overlaps with at least a part of a n-th scan line and a (n+1)-th scan line adjacent to the n-th scan line, wherein each of the scan lines (Reference Numeral 13 shown in Fig. 8) is formed in an inverted mesa shape in a sectional view to electrically separate the pixel electrode on each of the scan lines from the pixel electrode provided between the scan lines.

[0032]

[Effect]

Fig. 1 is a view illustrating a principle configuration and its effect according to a first embodiment of the invention. Fig. 1(a) is a circuit diagram conceptually illustrating the principle configuration. Fig. 1(b) is a view illustrating each voltage waveform to illustrate the effect.

[0033]

See Fig. 1(a).

A signal voltage V_{dn} 7 is applied from a signal line 4 to a pixel electrode 2 constituting one electrode of a pixel capacitance 1 through switching means 3 such as a TFT, and a common potential (opposite potential) V_{COM} is applied from a common power source to a division counter electrode 5 constituting the other electrode of the pixel capacitance 1 through switching means 6 such as a TFT. In this case, as described in Fig. 12, a parasitic capacitance C_{Pn} 9 is formed between the n-th signal line 4 and the pixel electrode 1 and a parasitic capacitance C_{Pn+1} 10 is formed between the (n+1)-th signal line 4 and the pixel electrode 1, respectively. At this time, a signal voltage V_{dn} 7 and a signal voltage V_{dn+1} 8 are applied to the parasitic capacitance C_{Pn} 9 and the parasitic capacitance C_{Pn+1} 10, respectively.

[0034]

See Fig. 1(b).

At this time, the switching means 3 is turned on while

the switching means 6 is turned on, the pixel capacitance 1 is applied and charged with the signal voltage V_{dn} 7, and then the switching means 3 is turned off. Subsequently, when the signal voltage V_{dn} 7 and the signal voltage V_{dn+1} 8 vary, in the known configuration in the state where the switching means 6 is turned on, the liquid crystal voltage decreases by ΔV_P in accordance with the variations in the signal voltage V_{dn} 7 and the signal voltage V_{dn+1} 8 because of the same reason described in Fig. 12.

[0035]

However, at this time, like the invention, since the switching means 6 is turned on only when the switching means 3 is turned on, the division counter electrode 5 is in a floating state at the time the signals V_{dn} and V_{dn+1} vary. Accordingly, the movement of the charge does not occur. Thus, since the pixel potential does not vary, the liquid crystal voltage does not vary, and thus a speck of brightness does not occur.

[0036]

Next, like other embodiments, since at least one stripe-shaped counter electrode is provided for one or more pixel on the scan line, and an application period of the scan voltage applied to the stripe-shaped counter electrode is set as a product of the number of scan lines grouped by the stripe-shaped counter electrode and one horizontal period, it is possible to remarkably decrease the number of elements for

switching the counter electrode, and thus it is possible to simplify a manufacture and drive of the apparatus.

[0037]

Since a bus line which is opposite the signal line and which is capacitive-coupled to the pixel electrode with the pixel electrode interposed therebetween is provided, and a signal with polarity opposite to that of a signal, which is applied to the signal line, is applied to the bus line, the voltage variation caused by the parasitic capacitance is offset because of the reason described in Fig. 13, and thus it is possible to prevent the variation in the liquid crystal voltage.

[0038]

Since a conductive thin film which is disposed between the pixel electrode and at least one of the n-th signal line and the (n+1)-th signal line to be capacitive-coupled to the pixel electrode, and a signal with polarity opposite to that of a signal, which is applied to each of the signal lines on the opposite side to a side where the conductive thin film is provided, is applied to the conductive thin film, the voltage variation caused by the parasitic capacitance is reduced, and thus it is possible to reduce the variation in the liquid crystal voltage.

[0039]

Since the signal line is coated with a high-resistance thin film, the parasitic capacitance is connected to the pixel

capacitance through a high resistance component. Accordingly, the waveform of the signal voltage becomes dull, and thus it is possible to reduce the variation in the liquid crystal voltage.

[0040]

Since the signal line is formed in an inverted mesa shape in a sectional view, the pixel electrode on the signal line which causes the parasitic capacitance is electrically separated from the pixel electrode between the signal lines, and thus it is possible to prevent the variation in the liquid crystal voltage. Additionally, since a conductive film is provided below the signal line, a difference in level of step increases, and thus a cutoff easily occur.

[0041]

Since the scan line is formed in an inverted mesa shape in a sectional view, the pixel electrode on the scan line is electrically separated from the pixel electrode between the scan lines, and thus the voltage variation which causes the variation in the scan voltage is prevented. Accordingly, it is possible to reduce the variation in the liquid crystal voltage.

[0042]

[Embodiments]

Fig. 2 is a view illustrating a first embodiment of the invention. Fig. 2(a) is a perspective view in which a part

of an active matrix type liquid crystal display device is enlarged and the part is perspectively shown. Fig. 2(b) is a sectional view illustrating pixel units of the active matrix type liquid crystal display device taken along a plane surrounded by A-B-C-D shown in Fig. 2(a).

[0043]

See Figs. 2(a) and 2(b).

First, on a TFT substrate 11 formed of an insulation substrate such as a glass substrate, signal lines 12 and scan lines 13 are disposed so as to intersect each other with a first interlayer insulation film 26 such as a SiO_2 film interposed therebetween, and a polycrystalline silicon layer connected to the signal lines 12 and gate electrodes 14 connected to the scan lines are provided. Accordingly, staggered type TFTs for switching pixels are formed. Additionally, a polycrystalline silicon film is first laminated, and then the gate electrodes 14 may be simultaneously patterned at the time of patterning the scan lines 13.

[0044]

Subsequently, a second interlayer insulation film 27 such as a SiO_2 film is provided thereon to cover the signal lines 12, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12 of the pixel and the signal line 12

of the adjacent pixel is formed.

[0045]

Meanwhile, on an opposite substrate 19 opposite the TFT substrate 11, a TFT which is opposite the pixel on the TFT substrate 11 one to one is disposed. The configuration of the TFT is basically the same as that of the TFT on the TFT substrate 11. A different point is that signal lines 20 and scan lines 21 are formed of a conductive film such as ITO, and each division counter electrode 25 is formed so as not to be disposed on the signal lines 20.

[0046]

That is, first, on an opposite substrate 19, the signal lines 20 and the scan lines 21 formed of a transparent conductive film such as ITO are provided thereon to intersect each other with a first interlayer insulation film 28 such as a SiO_2 film interposed therebetween, and a polycrystalline silicon layer connected to the signal lines 20 and gate electrodes 22 connected to the scan lines are provided thereon. Accordingly, TFTs for switching pixels are formed. Additionally, in this case, the polycrystalline silicon film is first laminated, and then the gate electrodes 22 may be simultaneously patterned at the time of patterning the scan lines 21.

[0047]

Subsequently, a second interlayer insulation film 29 such as a SiO_2 film is provided thereon to cover the signal lines

20, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon. Accordingly, each division counter electrode 25 of which a part is not disposed on the signal lines 20 is formed.

[0048]

Next, a method of driving the liquid crystal display device will be described. First, an equivalent signal (on period = 1 horizontal period) to that applied to the scan lines 13 on the TFT substrate 11 is applied to the scan lines 21 on the opposite substrate 19. Subsequently, in order to remove an influence of a parasitic capacitance between a gate and a source of the TFT on the opposite substrate 19, a common voltage V_{COM}, which is defined by the following expression, is applied to the signal lines 20.

$$V_{COM} = [C_{GS} / (C_{GS} + C_{pix})] \times \Delta V_G$$

where, C_{GS}: the parasitic capacitance between the gate and source of the TFT on the opposite substrate 19.

ΔV_G : an amplitude of the scan signal

[0049]

Accordingly, the division counter electrodes 25 disposed on the opposite substrate 19 are applied with the V_{COM} during a period in which the pixels are charged, and are floated during a holding period. As described in Fig. 1, even when the potential of the signal lines 12 on the TFT substrate 11 is changed, a liquid crystal voltage is maintained at the constant value

without a case where the liquid crystal voltage is changed, and thus brightness is not changed. Accordingly, a speck of brightness does occur.

[0050]

Additionally, in this case, as a semiconductor layer forming the TFT, polycrystalline silicon of which carrier mobility (in this case, electron mobility) is better than that of amorphous silicon is used. Accordingly, it is possible to integrate a driving circuit, which is used to generate the voltage V_{COM}, and a scan circuit into the opposite substrate 19.

[0051]

Next, a second embodiment of the invention in which a stripe-shaped counter electrode is used as a division counter electrode will be described with reference of Fig. 3.

See Figs. 3(a) and 3(b).

All pixels arranged in one scan-line direction provided on the TFT substrate 11 are referred to as one block, and one stripe-shaped counter electrode 32 for a plurality of scan-line blocks (in the drawing, five blocks) is provided on the opposite substrate 19. One switching element (not shown) such as a polycrystalline silicon TFT is provided for the one stripe-shaped counter electrode 32.

[0052]

In the driving of the liquid crystal display device, as

shown in Fig. 3(a), a scan signal 33 with a pulse width of an on period t of five times one horizontal period is applied to the one stripe-shaped counter electrode 32 so as to be synchronized with a scan signal from a scan circuit (gate driver) 31 for the pixel. Additionally, Reference Numeral 30 denotes a signal circuit (data driver) for the pixel. In this case, the advantage of reducing the speck of brightness is slightly reduced, but it is possible to remarkably decrease the number of the division counter electrodes and the number of TFTs compared with the first embodiment. Accordingly, the manufacture is easy and the manufacture yield is improved.

[0053]

Additionally, in the drawing, one counter electrode is provided for the five blocks, but is not limited to the five blocks. An arbitrary scan-line block is grouped, and then one stripe-shaped counter electrode may be provided for the grouped scan-line block. In this case, the on period of the scan signal applied to the stripe-shaped counter electrode may be the number of the grouped scan-line blocks × one horizontal period.

[0054]

Next, a third embodiment of the invention in which amorphous silicon layer is used as a semiconductor layer will be described with reference to Fig. 4.

See Fig. 4.

In the embodiment, the configuration of a display portion

of the TFT substrate 11 and the counter electrode portion of the opposite substrate 19 is the same as that in the first embodiment. However, it is different from the first embodiment in that the switching TFT is formed of amorphous silicon. Accordingly, the configuration of the driving circuit is different, but the operation and the effect are the same as those in the first embodiment.

[0055]

That is, since an operation speed of the TFT using the amorphous silicon is late, it is necessary to provide the signal circuit and the scan circuit in an external circuit formed of a transistor using other semiconductors. A signal-side TAB 34, a scan-side TAB 35, and an opposite substrate scan TAB 37 are provided so as to connect the signal line and the scan line between the external circuit and the TFT substrate 11 or the scan line of the opposite substrate 19. Additionally, a signal power source 36 on the side of the opposite substrate is provided on the TFT substrate 11 so as to apply the common voltage V_{COM} to the signal line on the side of the opposite substrate 19.

[0056]

In this case, in the same manner as the second embodiment, the counter electrode may be formed in a stripe shape. At this time, an opposite substrate scan TAB and an external scan circuit having a configuration in accordance with the number of the stripe-shaped counter electrodes may be provided.

[0057]

Next, a fourth embodiment of the invention will be described with reference to Fig. 5. Additionally, Fig. 5(a) is a sectional view illustrating a TFT substrate of the pixel units. Fig. 5(b) is an equivalent circuit to that of the fourth embodiment.

[0058]

See Fig. 5(a).

First, on the TFT substrate 11 formed of an insulation substrate such as a glass substrate, the signal lines 12 and the scan lines are provided thereon so as to intersect each other with the first interlayer insulation film 26 such as a SiO_2 film. Additionally, the polycrystalline silicon layer connected to the signal lines 12 and the gate electrodes connected to the scan lines are formed at an appropriate time in accordance with the type of the liquid crystal display device.

[0059]

Subsequently, the second interlayer insulation film 27 such as a SiO_2 film is provided thereon to cover the signal lines 12, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12 of the pixel and the signal line 12 of the adjacent pixel is formed. Subsequently, a conductive film formed of Al is laminated thereon with a third

interlayer insulation film formed of a SiO_2 film interposed therebetween, and then a patterning is performed thereon. Accordingly, bus lines 40 which are opposite the signal lines 12 with the pixel electrodes 17 interposed therebetween are formed.

[0060]

See Fig. 5(b).

In the n-th bus line 40, a signal (n bar in the drawing) which has a inverted phase to a signal (n) applied to the n-th signal line 12 is applied, and thus a variation in the liquid crystal voltage in accordance with the variation in the signal voltage applied to the n-th signal line 12 is offset by the principle described in Fig. 13. Additionally, in the (n+1)-th bus line 40, a signal (n+1 bar in the drawing) which has a inverted phase to a signal (n) applied to the (n+1)-th signal line 12 is applied in the same manner.

[0061]

In this case, when parasitic capacitances C'_{Pn} and C'_{Pn+1} formed by the bus lines and the pixel electrodes are the same as parasitic capacitances C_{Pn} and C_{Pn+1} formed by the signal lines and the pixel electrodes, a voltage with the same amplitude as that of the signal line may be applied to the bus line. Additionally, when the parasitic capacitances are different from each other, it is desirable to apply a signal having a relation which offsets the difference between the parasitic

capacitances.

[0062]

A fifth embodiment of the invention will be described with reference to Fig. 6(a).

See Fig. 6(a).

Fig. 6(a) is a sectional view illustrating the pixel units on the TFT substrate. First, on the TFT substrate 11 formed of an insulation substrate such as a glass substrate, the signal lines 12 and the scan lines are provided thereon so as to intersect each other with the first interlayer insulation film 26 such as a SiO_2 film. Additionally, the polycrystalline silicon layer connected to the signal lines 12 and the gate electrodes connected to the scan lines are formed at an appropriate time in accordance with the type of the liquid crystal display device.

[0063]

Subsequently, the second interlayer insulation film 27 such as a SiO_2 film is provided thereon to cover the signal lines 12. Subsequently, a conductive film formed of Al is laminated thereon with the second interlayer insulation film 27 formed of a SiO_2 film interposed therebetween, and then a patterning is performed thereon. Accordingly, a conductive thin film 41 is formed on one of fillets of the signal lines 12.

[0064]

Subsequently, a conductive film such as ITO is deposited

thereon with a fourth interlayer insulation film 42 formed of the same SiO_2 film interposed therebetween. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12 of the pixel and the signal line 12 of the adjacent pixel is formed.

[0065]

In this case, in the conductive thin film 41 formed on the fillet of the (n+1)-th signal line 12, a signal which has an inverted phase to the signal applied to the n-th signal line is applied. Similarly, the variation in the liquid crystal voltage in accordance with the variation in the signal voltage applied to the n-th signal line is offset by the principle described in Fig. 13.

[0066]

In the fifth embodiment described above, the conductive thin film 41 is provided on the (n+1)-th signal line 12, but may be provided on the n-th signal line 12 (the fillet on the opposite side in the drawing). In this case, in the conductive thin film 41 provided in the fillet of the n-th signal line 12, a signal which has an inverted phase to a signal applied to the (n+1)-th signal line is applied. Accordingly, the variation in the liquid crystal voltage in accordance with the variation in the signal voltage applied to the (n+1)-th signal line is offset by the principle described in Fig. 13.

[0067]

A sixth embodiment of the invention will be described with reference to Fig. 6(b).

See Fig. 6(b).

Fig. 6(b) is a sectional view illustrating the pixel units on the TFT substrate. First, on the TFT substrate 11 formed of an insulation substrate such as a glass substrate, the signal lines 12 and the scan lines are provided thereon so as to intersect each other with the first interlayer insulation film 26 such as a SiO_2 Film. Additionally, the polycrystalline silicon layer connected to the signal lines 12 and the gate electrodes connected to the scan lines are formed at an appropriate time in accordance with the type of the liquid crystal display device.

[0068]

Subsequently, a thin film layer such as polycrystalline silicon of high resistance is laminated thereon so as to cover the signal lines 12, and then a patterning is performed to form a high-resistance thin film 43. Subsequently, a conductive film such as ITO is deposited thereon with the second interlayer insulation film 27 such as a SiO_2 film interposed therebetween. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12 of the pixel and the signal line 12 of the adjacent pixel is formed.

[0069]

In this case, a parasitic capacitance formed between both the signal line 12 and the pixel electrode 17 is connected to a pixel capacitance through a serial connection resistance caused by the high-resistance thin film 43. Accordingly, a voltage waveform at the time the voltage varies becomes dull, and thus it is possible to reduce the variation in the liquid crystal voltage. Additionally, in this case, the high-resistance thin film 43 is formed of polycrystalline silicon, but is not limited to the polycrystalline silicon. The high-resistance thin film may be formed of amorphous silicon, other semiconductor thin films, or a metal thin film of high resistance such as NiCr.

[0070]

Next, a seventh embodiment of the invention will be described with reference to Fig. 7(a).

See Fig. 7(a).

Fig. 7(a) is a sectional view illustrating the pixel units on the TFT substrate. First, on the TFT substrate 11 formed of an insulation substrate such as a glass substrate, the signal lines 12 with a revere-mesa shape in a sectional view are provided thereon to intersect the scan lines with the first interlayer insulation film 26 such as a SiO_2 film interposed therebetween. Additionally, the revere-mesa shape is formed by controlling an etching condition such as etchant at the time the signal line is patterned. Additionally, the polycrystalline silicon

layer connected to the signal lines 12 and the gate electrodes connected to the scan lines are formed at an appropriate time in accordance with the type of the liquid crystal display device.

[0071]

Subsequently, the second interlayer insulation film 27 such as a SiO_2 film is laminated thereon, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12 of the pixel and the signal line 12 of the adjacent pixel is formed. In this case, a step coverage of the conductive film such as ITO is poor, and thus in an acute fillet of the signal line 12 with an inverted mesa shape in a sectional view, a thinning or a cutoff of the pixel electrode film occurs.

[0072]

Accordingly, most of pixel electrodes 17 existing between the signal lines 12 are electrically separated from the pixel electrodes 17 existing on the signal lines 12 forming the parasitic capacitance and cutoff portions 44 or high resistance portions 45 caused by the thinning. Thus, the voltage variation in the signal lines 12 does not affect a pixel potential through the pixel electrodes 17 existing on the signal lines 12. Accordingly, it is possible to prevent the variation in the liquid crystal voltage.

[0073]

Next, an eight embodiment of the invention will be described with reference to Fig. 7(b).

See Fig. 7(b).

Fig. 7(b) is a sectional view illustrating the pixel units on the TFT substrate. First, on a TFT substrate 11 formed of an insulation substrate such as a glass substrate, a conductive film 46 is provided along a direction intersecting the scan lines, and then a conductive layer is laminated thereon with the first interlayer insulation film 26 such as a SiO_2 film interposed therebetween. Subsequently, a patterning is performed thereon, and thus the signal lines 12 with an inverted mesa shape in a sectional view are formed on the conductive film 46. Additionally, the inverted mesa shape is formed by controlling an etching condition such as etchant at the time the signal lines are patterned. Additionally, the polycrystalline silicon layer connected to the signal lines 12 and the gate electrodes connected to the scan lines are formed at an appropriate time in accordance with the type of the liquid crystal display device.

[0074]

Subsequently, the second interlayer insulation film 27 such as a SiO_2 film is laminated thereon, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the signal line 12

of the pixel and the signal line 12 of the adjacent pixel is formed. In this case, a step coverage of the conductive film such as ITO is poor, and thus a difference in level of step is emphasized by the conductive film 46. Additionally, in the fillet of the signal line 12 with an inverted mesa shape in a sectional view, the thinning or the cutoff of the pixel electrode film easily occurs.

[0075]

Accordingly, most of pixel electrodes 17 existing between the signal lines 12 are electrically separated from the pixel electrodes 17 existing on the signal lines 12 forming the parasitic capacitance and cutoff portions 44 or high resistance portions 45 caused by the thinning. The voltage variation in the signal lines 12 does not affect a pixel potential through the pixel electrodes 17 existing on the signal lines 12. Accordingly, it is possible to prevent the variation in the liquid crystal voltage.

[0076]

Additionally, the conductive film 46 in the eighth embodiment may be formed by patterning from a conductive layer for forming the scan lines, that is, the conductive layer in the same layer as the scan lines. In this case, in order to prevent a short circuit between the scan lines, it is necessary to perform the patterning in an appropriate shape. Additionally, a difference in level of step is emphasized by the conductive

film 46, and thus the cutoff easily occurs. Therefore, it is not necessary for the signal lines 12 provided on the conductive film 46 to have an inverted mesa shape in a sectional view, but a rectangular shape or a mesa shape may be used.

[0077]

A ninth embodiment of the invention will be described with reference to Fig. 8. In addition, Fig. 8(a) is a top view illustrating a pixel configuration on the side of the TFT substrate (in the drawing, one pixel is shown). Fig. 8(b) is a sectional view taken along the dashed line B-B' shown in Fig. 8(a).

[0078]

See Figs. 8(a) and 8(b).

First, on the TFT substrate 11 formed of an insulation substrate such as a glass substrate, the scan lines 13 with an inverted mesa shape in a sectional view are provided thereon along a direction intersecting the signal lines 12. Subsequently, a conductive layer such as Al is laminated thereon with the first interlayer insulation film 26 interposed therebetween, and then a patterning is performed thereon. Accordingly, the signal lines 12 are formed thereon. Additionally, the revere-mesa shape is formed by controlling an etching condition such as etchant at the time the scan line is patterned. Additionally, the polycrystalline silicon layer connected to the signal lines 12 and the gate electrodes

connected to the scan lines are formed at an appropriate time in accordance with the type of the liquid crystal display device.

[0079]

Subsequently, the second interlayer insulation film 27 such as a SiO_2 film is laminated thereon, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon Accordingly, each pixel electrode 17 of which a part is disposed between both the scan line 13 of the pixel and the scan line 13 of the adjacent pixel is formed. In this case, a step coverage of the conductive film such as ITO is poor, and thus in the fillet of the scan line 13 with an inverted mesa shape in a sectional view, the thinning or the cutoff of the pixel electrode film occurs.

[0080]

Accordingly, most of pixel electrodes 17 existing between the scan lines 13 are electrically separated from the pixel electrodes 17 existing on the scan lines 13 forming the parasitic capacitance and cutoff portions 44 or high resistance portions 45 caused by the thinning. The voltage variation in the scan lines 13 does not affect a pixel potential through the pixel electrodes 17 existing on the scan lines 13. Accordingly, it is possible to prevent the variation in the liquid crystal voltage.

[0081]

Next, a tenth embodiment of the invention will be described

with reference to Fig. 9. Additionally, Fig. 9(a) is a top view illustrating the pixel configuration on the TFT substrate (in the drawing, one pixel is shown). Fig. 9(b) is a sectional view taken along the dashed line C-C' shown in Fig. 9(a).

[0082]

See Figs. 9(a) and 9(b).

First, on the TFT substrate 11 formed of an insulation substrate such as a glass substrate, the scan lines 13 with an inverted mesa shape in a sectional view and auxiliary capacitance bus lines 47 with a rectangular shape in a sectional view are formed along the direction intersecting the signal lines 12. Subsequently, a conductive layer such as Al is laminated thereon with the first interlayer insulation film 26 such as a SiO_2 film interposed therebetween. Subsequently, a patterning is performed thereon, and thus the signal lines 12 are formed.

[0083]

Additionally, the inverted mesa shape is formed by controlling an etching condition such as etchant at the time the scan lines 13 are patterned. When the condition of patterning the scan lines 13 and the auxiliary capacitance bus lines 47 is changed, a difference in the sectional shape occurs. Additionally, the polycrystalline silicon layer connected to the signal lines 12 and the gate electrodes connected to the scan lines are formed at an appropriate time in accordance with

the type of the liquid crystal display device.

[0084]

Subsequently, the second interlayer insulation film 27 such as a SiO_2 film is laminated thereon, and then a conductive film such as ITO is deposited thereon. Subsequently, a patterning is performed thereon. Accordingly, each pixel electrode 17 of which a part is disposed between both the scan line 13 of the pixel and the scan line 13 of the adjacent pixel is formed. In this case, a step coverage of the conductive film such as ITO is poor, and thus in an acute fillet of the scan line 13 with an inverted mesa shape in a sectional view, the thinning or the cutoff of the pixel electrode film occurs. However, in a right-angle or obtuse-angle fillet of the auxiliary capacitance bus line 47 with a substantially rectangular shape in a sectional view, the thinning or the cutoff of the pixel electrode film does not occur.

[0085]

Accordingly, most of pixel electrode 17 existing between the scan lines 13 function as integrated pixel electrodes without the thinning or the cutoff of the pixel electrode film in the fillet of the auxiliary capacitance bus line 47, and are electrically separated from the pixel electrodes 17 existing on the scan lines 13 forming the parasitic capacitance and cutoff portions 44 or high resistance portions 45. Thus, the voltage variation in the scan lines 13 does not affect a pixel potential

through the pixel electrodes 17 existing on the scan lines 13. Accordingly, it is possible to prevent the variation in the liquid crystal voltage.

[0086]

Additionally, the auxiliary capacitance bus lines 47 in the tenth embodiment are provided to prevent the variation in the liquid crystal voltage in accordance with a signal applied to the signal lines. The auxiliary capacitance bus lines 47 may be formed by performing a patterning from a conductive layer for forming the scan lines 13.

[0087]

Additionally, in the fourth embodiment to the tenth embodiment, the configuration of the counter electrode is not described, but the undesirable transformation voltage variation caused by the parasitic capacitance is prevented by considering the configuration on the TFT substrate. Like the known active matrix type liquid crystal display device, an integrated counter electrode with a beta shape may be used. However, in order to more securely prevent the undesirable transformation voltage variation, the division counter electrode in the first embodiment to the third embodiment may be used.

[0088]

Additionally, in the embodiments, as the interlayer insulation film, the SiO_2 film is used, but a transparent

insulation film relative to visual light may be used. For example, a silicon nitride film may be used.

[0089]

Additionally, in the embodiments, as the switching element, the staggered type TFT is used, but the switching element is not limited to the staggered type TFT. A TFT having a configuration in which the gate electrodes are directly formed on the TFT substrate and then the semiconductor layer is laminated thereon may be used. In this case, the scan lines are first laminated, and then the polycrystalline silicon film is laminated thereon. Subsequently, the signal lines are formed thereon with the first interlayer insulation film interposed therebetween.

[0090]

[Advantage of the Invention]

According to the invention, in order to prevent a variation in a liquid crystal voltage in accordance with a variation in a voltage of signal lines or scan lines, a counter electrode opposite a pixel electrode is provided as a division counter electrode. A scan signal in accordance with a scan signal which is applied to gate electrodes of TFTs connected to the opposite pixel electrodes is applied to the division counter electrodes. Bus lines which are opposite the signal lines with the pixel electrode interposed therebetween and which are capacitive-coupled to the pixel electrode are provided. A

signal which has polarity opposite to that of the signal applied to the signal lines is applied to the bus lines. Alternatively, a sectional shape of the signal line or the scan line is formed in an inverted mesa shape, and thus the pixel electrodes on the signal lines or the scan lines are electrically separated from the pixel electrodes on the signal lines or the scan lines. Accordingly, it is possible to remove a speck of brightness caused by a parasitic capacitance, and thus it is possible to provide an excellent aperture-ratio active matrix type liquid crystal display device with high resolution.

[Brief Description of the Drawings]

[Fig. 1] Fig. 1 is a view illustrating a principle configuration and its effect according to a first embodiment of the invention.

[Fig. 2] Fig. 2 is a view illustrating the first embodiment of the invention.

[Fig. 3] Fig. 3 is a view illustrating a second embodiment of the invention.

[Fig. 4] Fig. 4 is a view illustrating a third embodiment of the invention.

[Fig. 5] Fig. 5 is a view illustrating a fourth embodiment of the invention.

[Fig. 6] Fig. 6 is a view illustrating fifth and sixth embodiments of the invention.

[Fig. 7] Fig. 7 is a view illustrating seventh and eighth

embodiments of the invention.

[Fig. 8] Fig. 8 is a view illustrating a ninth embodiment of the invention.

[Fig. 9] Fig. 9 is a view illustrating a tenth embodiment of the invention.

[Fig. 10] Fig. 10 is a top view illustrating a pixel configuration of a known liquid crystal display device.

[Fig. 11] Fig. 11 is a view illustrating a pixel configuration of a known aperture-ratio liquid crystal display device with high resolution.

[Fig. 12] Fig. 12 is a view illustrating an operation of the known aperture-ratio liquid crystal display device with high resolution.

[Fig. 13] Fig. 13 is a view illustrating a case where a signal voltage of an adjacent signal line is a inverted phase.

[Fig. 14] Fig. 14 is a view illustrating a case where the signal voltage of the adjacent signal line is the same phase.

[Description of Reference Numerals and Signs]

1: PIXEL CAPACITANCE

2: PIXEL ELECTRODE

3: SWITCHING MEANS

4: SIGNAL LINE

5: DIVISION COUNTER ELECTRODE

6: SWITCHING MEANS

7: SIGNAL VOLTAGE V_{dn}

8: SIGNAL VOLTAGE V_{dn+1}

9: PARASITIC CAPACITANCE C_{Pn}

10: PARASITIC CAPACITANCE C_{Pn+1}

11: TFT SUBSTRATE

12: SIGNAL LINE

13: SCAN LINE

14: GATE ELECTRODE

15: DRAIN

16: SOURCE

17: PIXEL ELECTRODE

18: LIQUID CRYSTAL

19: OPPOSITE SUBSTRATE

20: SIGNAL LINE

21: SCAN LINE

22: GATE ELECTRODE

23: DRAIN

24: SOURCE

25: DIVISION COUNTER ELECTRODE

26: FIRST INTERLAYER INSULATION FILM

27: SECOND INTERLAYER INSULATION FILM

28: FIRST INTERLAYER INSULATION FILM

29: SECOND INTERLAYER INSULATION FILM

30: SIGNAL CIRCUIT

31: SCAN CIRCUIT

32: STRIPE SHAPED COUNTER ELECTRODE

33: SCAN SIGNAL

34: SIGNAL-SIDE TAB

35: SCAN-SIDE TAB

36: OPPOSITE SUBSTRATE-SIDE SIGNAL POWER SOURCE

37: OPPOSITE SUBSTRATE-SIDE SCAN TAB

38: BOUNDARY OF LIGHT SHIELDING FILM

39: THIRD INTERLAYER INSULATION FILM

40: BUS LINE

41: CONDUCTIVE THIN FILM

42: FOURTH INTERLAYER INSULATION FILM

43: HIGH-RESISTANCE THIN FILM

44: CUTOFF PORTION

45: HIGH-RESISTANCE PORTION

46: CONDUCTIVE FILM

47: AUXILIARY CAPACITANCE BUS LINE